# EXPERIMENT 6: HAZARDS AND GLITCHES

## PURPOSE

The purpose of this experiment is to consider the effect of glitches, caused by hazards, in combinational circuits.

## HAZARDS IN COMBINATIONAL CIRCUITS

Assume that a Boolean function, F, can be expressed as a sum of two product terms, F1 and F2. Both these terms might be functions of the same logical variable, A, the value of which is changing. Let the value of A before the change be denoted by A and, after the change, by A\*.

Consider the expressions:

 F(A) = F1(A) + F2(A)

 F(A\*) = F1(A\*) + F2(A\*)

A static-1 hazard exits if F1(A)=0 and F2(A)=1, but F1(A\*)=1 and F2(A\*)=0. In other words, if the value of the Boolean expression F before and after the change is 1, but the 1 is caused by two different product terms that change due to the change in A. In the circuit implementing F, the gate and wire delays may be such that F1 and F2 are simultaneously 0. This will cause F to become 0 for a short time, in which case, the static-1 hazard in the function results in a glitch in the circuit.

In general, a hazard is the possibility of an unwanted transient (spike or glitch). In a particular circuit implementing the function, a glitch may or may not occur depending the actual delays in the circuit.

***As part of your preparation for this experiment, you are expected to read section 8.4 in the textbook.***

## PRELAB

1. Consider the combinational circuit shown in Figure 8.8-a in your textbook. This circuit implements the Boolean function F = AB’ + BC, where A, B and C are the inputs.
2. Draw the logic diagram for the circuit using NAND gates and inverters, if needed. (The circuit must match the equation as given.)
3. Construct the Karnaugh map for the function F.
4. Analyze the circuit to determine if it contains static-1 hazards. (Assume only one input, A, B or C, can change at a time.) Determine whether these hazards could cause glitches for some combination of gate delays. Construct a timing diagram to illustrate this behavior.
5. Breadboard the circuit from 1 above. (Note that in the procedure below you are asked to insert two inverters in series in different paths of the circuit and, also, to modify the circuit so that it is free of glitches. You may want to breadboard the circuit so that these modifications are easy.)

## PROCEDURE

Before performing the procedures listed below, read the report section of the experiment to assure you make all required measurements and record all required data.

1. Use your breadboard of the original circuit (Figure 8.8-a in the textbook) to measure the length of each glitch using the pulse generator and the oscilloscope. Obtain a timing diagram for the transition High -> Low and for the transition Low -> High of the input that causes the hazard.
2. Modify the original circuit by inserting 2 inverters after the NAND gate that has inputs B and C. Breadboard the circuit and measure the length of each glitch using the pulse generator and the oscilloscope. Obtain a timing diagram for the transition High -> Low and for the transition Low -> High of the input that causes the hazard. What do you observe? Does this circuit contain more glitches than the original (in 1. above)?
3. Now modify the original circuit so that it contains no hazards. Obtain a timing diagram for the transition High -> Low and for the transition Low -> High of the input that caused the hazard in the original circuit (part 1. above). Do you observe any glitches now?

**EXPERIMENT 6--HAZARDS AND GLITCHES**

 **FINAL REPORT**

**I. *Hazards in the original circuit (Figure 8 .8-a in the textbook).***

a) Sketch the timing diagrams obtained in part 1 of the procedure. Clearly indicate the glitches.



*Low -> High*



*High -> Low*

b) What is the length of each glitch measured in part 1 of the procedure?

**II. *Hazards in the modified circuit with NOT gates.***

a) Sketch the timing diagrams obtained in part 2 of the procedure. Clearly indicate the glitches.



*Low -> High*



*High -> Low*

b) What is the length of each glitch measured in part 2 of the procedure?

**III. *Elimination of hazards (Part 3 of the procedure).***

a) Draw the modified circuit that eliminates the hazard in the space below.

b) Sketch the timing diagrams obtained in part 3 of the procedure.



*Low -> High*



*High -> Low*

c) Explain why the glitches disappeared.