

Synthesis of Correlated Bit Streams for Stochastic Computing

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Abstract—Stochastic computing using simple logic circuits requires significantly less area and consumes less power compared to traditional computing systems. These circuits are also inherently fault-tolerant. The main drawbacks of these systems include long latency and inexactness in computing. The deviation from exact values increases as the correlation among inputs increases. In many applications, outputs from different sensors may be correlated. Thus, testing correctness of stochastic computing circuits requires generation of correlated stochastic bit streams. While uncorrelated bit streams can be generated using linear feedback shift registers (LFSRs), generation of correlated stochastic bit streams has not yet been fully investigated. This paper presents a general approach to synthesize correlated stochastic bit streams for specified probabilities and specified correlation coefficients. Generation of N correlated stochastic bit streams requires N probabilities and $2^N - N - 1$ correlation coefficients. Using N LFSRs, N uncorrelated stochastic bit streams are first generated. The N correlated bit streams are then generated one at a time using conditional marginal probabilities. The method is illustrated for generating two and three correlated bit streams. The area and power overheads for two correlated bit streams are 9.09% and 2.12%, respectively, and for three correlated bit streams are 21.03% and 4.80%, respectively. The generated sequences are applied to simple stochastic logic gates and the probability density functions (pdfs) of the outputs are derived. It is shown that these match with the theoretical pdfs of the outputs.

Keywords—Stochastic computing, stochastic combinational logic, bit-level correlation, correlated stochastic sequences, error estimation, synthesis.

I. INTRODUCTION

Stochastic Computing (SC) was proposed in 1967 by Gaines [1] [2]. SC was proposed as an alternative approach to binary computing. Gaines proposed stochastic representation in two formats, unipolar and bipolar. The unipolar format is used for unsigned numbers within the range of $[0, 1]$, whereas signed numbers correspond to the range of $[-1, 1]$ in the bipolar format. In the unipolar format, a real number x is represented by a stochastic stream of bits X , where

$$x = P(X = 1) = P(X).$$

For example, in a stochastic sequence with 256 bits, if 25 bits are 1, then the real number described by the sequence is 25/256. In the bipolar format,

$$x = 2P(X = 1) - 1 = 2P(X) - 1.$$

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In this paper, we first present synthesis of correlated stochastic sequences for the unipolar representation of stochastic computing and then extend our work to bipolar format.

Computing using stochastic logic requires significantly less hardware compared to traditional binary arithmetic. However, these circuits suffer from significant increase in latency. This is because the number of bits used to represent a number is typically very large. For example, a 10-bit binary number can represent 1024 levels. To achieve the same resolution, a stochastic number should be represented using 1024 bits. The stochastic computing systems are ideal for low-speed applications such as neural networks [3], cyber-physical systems operating at very low rates, and biomedical applications. Stochastic logic gates compute an approximate value of the result, as opposed to the exact value. In many applications, such as machine learning, where a decision is made based on a thresholding operation, the decisions may not be affected by approximate computing. Stochastic computing is also exploited for decoding of error-correcting codes (ECC) [4] [5]. Another main advantage of stochastic computing is its inherent tolerance to faults in CMOS circuits [6].

The stochastic bit stream is represented using a string of 1s and 0s where each bit is assumed to be independent of the other bits. Parker and McCluskey derived closed-form expressions for stochastic logic outputs for uncorrelated inputs [7]. Qian *et al.* have proposed synthesis of logic gates to compute specified probabilities from uncorrelated bit streams [8] [9]. However, the bit-level correlation between the two inputs to a stochastic logic gate affects the expected value of the output. Recently, Alaghi and Hayes have introduced the notion of *stochastic correlation* and have proposed a method to generate correlated bit streams using probabilistic transfer matrices [10]. In contrast, the proposed work presents a method to generate correlated bit streams using the traditional Pearson correlation. Although the Pearson correlation coefficient, ρ , lies between -1 and 1, the ρ of two stochastic bit streams is restricted to a narrower range; this range is dependent on the expected values of the stochastic inputs. It was described in [11] that two correlated bit streams can be generated for specified probabilities and correlation coefficients and this paper expands the results of [11].

This paper makes two key contributions. First, closed-form expressions are derived for mean and variance of a stochastic output as functions of the input probabilities and the spatial correlation between the inputs. To prove the theoretical expressions by simulations, it is necessary to generate correlated bit

streams for a specified correlation. The second contribution of this paper is a novel approach to generate correlated stochastic bit streams given specified probabilities and correlation coefficients. Finally the validity of the theoretical expressions is demonstrated through simulations of stochastic logic gates using correlated bit streams.

This paper is organized as follows. In Section II closed-form expressions for outputs of stochastic logic gates with correlated inputs are derived. Sections III and IV, respectively, present approaches to synthesize two and three correlated stochastic bit streams from uncorrelated bit streams. Section V extends our work from stochastic unipolar format to bipolar format. Section VI tests the synthesis circuit to generate correlated stochastic bit streams and stochastic logic gates with correlated inputs. The hardware complexity and power consumption of synthesized circuits are also presented in this section. Finally, some conclusions are given in Section VII.

II. ANALYSIS OF STOCHASTIC LOGIC WITH CORRELATED INPUTS

In the implementation of functionalities using stochastic computing, independent or uncorrelated input signals are always required to guarantee the accuracy. We first analyze the output error of stochastic combinational logic under the assumption of uncorrelated inputs. Consider the output bit stream Y of an arbitrary stochastic combinational logic in unipolar format. Each bit Y_i can be represented as an independent identically distributed (i.i.d.) Bernoulli random variable with probability of one equal to p_Y . Assume that $P(Y)$ is the number represented by the stochastic bit stream Y . The value of $P(Y)$ is given by:

$$P(Y) = \frac{\sum_{i=1}^N Y_i}{N}, \quad (1)$$

where N is the number of bits in the stochastic sequence. Since $P(Y)$ is the sum of N Bernoulli random variables, it can be describes as a binomial random variable with the variance:

$$\sigma^2 = \frac{p_Y(1-p_Y)}{N}. \quad (2)$$

The variance is maximum at $p_Y = 0.5$ and minimum at $p_Y = 0$ or $p_Y = 1$. The variance of stochastic logic output actually reflects the computational error. Therefore, when $p_Y = 0.5$, the computational error is maximum while the minimum error is given at $p_Y = 0$ or $p_Y = 1$. The equation (2) also explains the fact that the computational error is reduced with the increase in the number of bits N .

A. Stochastic combinational logic with two correlated input sequences

Correlation in input bit streams alters the expected output of a stochastic logic circuit. The first example is a multiplication of two unipolar stochastic numbers using an AND gate as shown in Fig. 1. Let X_1 and X_2 denote the bits of two input stochastic sequences. The probabilities of the two bit streams, denoted as p_1 and p_2 , are $1/2$ and $1/3$. The stochastic bit stream consists of 6 bits. Let Y represent the output. If X_1 and X_2 are uncorrelated, the output probability is given by

$$E(Y) = E(X_1 X_2) = p_1 p_2. \quad (3)$$

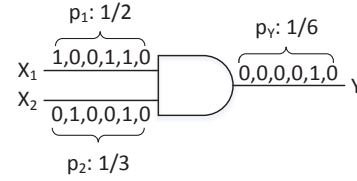


Fig. 1: The unsigned stochastic multiplication implemented using an AND gate.

In this example the output value is $1/6$. If two inputs are correlated at the bit-level, the expected value of the output will change. Consider the Pearson correlation coefficient of two binary variables X_1 and X_2 :

$$\begin{aligned} \rho_{12} &= \frac{\text{cov}(X_1, X_2)}{\sigma_1 \sigma_2} = \frac{E(X_1 X_2) - E X_1 E X_2}{\sigma_1 \sigma_2} \\ &= \frac{E(Y) - p_1 p_2}{\sigma_1 \sigma_2}, \end{aligned} \quad (4)$$

where the expected value of the stochastic input variable is given by $E X_i = p_i$ and the bit-level standard deviation is given by $\sigma_i = \sqrt{p_i(1-p_i)}$. Then the expected output of stochastic multiplication (AND operation) with two correlated input bit streams is derived as follows:

$$\begin{aligned} E(Y) &= p_1 p_2 + \rho_{12} \sigma_1 \sigma_2 \\ &= p_1 p_2 + \rho_{12} \sqrt{p_1 p_2 (1-p_1)(1-p_2)}. \end{aligned} \quad (5)$$

The computational error can be described in terms of ρ_{12} , p_1 and p_2 :

$$\begin{aligned} \text{err}(Y) &= E(Y) - p_1 p_2 \\ &= \rho_{12} \sqrt{p_1 p_2 (1-p_1)(1-p_2)}. \end{aligned} \quad (6)$$

Consider another example of the two-input OR gate. If the input signals X_1 and X_2 are uncorrelated, the expected value of the output Y is $p_1 + p_2 - p_1 p_2$, where p_1 and p_2 are probabilities of ones in X_1 and X_2 . Assume that X_1 and X_2 are correlated with correlation coefficient ρ , from equation (4), we obtain the expected value of the output as follows:

$$\begin{aligned} E(Y) &= E(X_1 + X_2 - X_1 X_2) \\ &= p_1 + p_2 - p_1 p_2 - \rho \sigma_1 \sigma_2. \end{aligned} \quad (7)$$

The expected output of any stochastic combinational logic with correlated input signals can be derived in a similar manner. Table I compares the expected values of the outputs of various two-input stochastic logic gates with uncorrelated and correlated inputs. Notice that the expected output of a MUX is unaffected by input correlation since we only consider the correlation of operands. The scaled addition is implemented using a MUX in stochastic computing. Let X_1 and X_2 denote the input signals, and X_3 represent the select signal. The expected value of output is given by:

$$\begin{aligned} E(Y) &= E(X_1 - X_1 X_3 + X_2 X_3) \\ &= p_1 - p_1 p_3 + p_2 p_3. \end{aligned} \quad (8)$$

where $E(X_i) = p_i$. Although the mean output is unaffected by correlation between X_1 and X_2 , it is affected by the correlation between the select signal, X_3 , and either or both input signals, X_1 or X_2 .

TABLE I: The expect values of output for various two-input stochastic logic gates with uncorrelated and correlated inputs.

Gate Type	uncorrelated inputs	correlated inputs (with correlation ρ)
AND	$p_1 p_2$	$p_1 p_2 + \rho \sigma_1 \sigma_2$
NAND	$1 - p_1 p_2$	$1 - p_1 p_2 - \rho \sigma_1 \sigma_2$
OR	$p_1 + p_2 - p_1 p_2$	$p_1 + p_2 - p_1 p_2 - \rho \sigma_1 \sigma_2$
NOR	$(1 - p_1)(1 - p_2)$	$1 - p_1 - p_2 + p_1 p_2 + \rho \sigma_1 \sigma_2$
XOR	$p_1 + p_2 - 2p_1 p_2$	$p_1 + p_2 - 2p_1 p_2 - 2\rho \sigma_1 \sigma_2$
XNOR	$1 - p_1 - p_2 + 2p_1 p_2$	$1 - p_1 - p_2 + 2p_1 p_2 + 2\rho \sigma_1 \sigma_2$
MUX (X_3 select signal)	$p_1 - p_1 p_3 + p_2 p_3$	$p_1 - p_1 p_3 + p_2 p_3$

B. Stochastic combinational logic with three correlated input sequences

When the number of inputs for a stochastic combinational logic is greater than two, the influence of correlation on expected output becomes more complex. Consider the unipolar stochastic multiplication of three inputs X_1 , X_2 and X_3 . The probabilities of ones in these sequences are given as following:

$$\begin{aligned} E(X_1) &= p_1 \\ E(X_2) &= p_2 \\ E(X_3) &= p_3. \end{aligned}$$

In this situation, the correlations of three inputs are required to be described using three pairwise correlations:

$$\begin{aligned} \rho_{12} &= \frac{\text{cov}(X_1, X_2)}{\sigma_1 \sigma_2} = \frac{E(X_1 X_2) - p_1 p_2}{\sigma_1 \sigma_2} \\ \rho_{23} &= \frac{\text{cov}(X_2, X_3)}{\sigma_2 \sigma_3} = \frac{E(X_2 X_3) - p_2 p_3}{\sigma_2 \sigma_3} \\ \rho_{13} &= \frac{\text{cov}(X_1, X_3)}{\sigma_1 \sigma_3} = \frac{E(X_1 X_3) - p_1 p_3}{\sigma_1 \sigma_3}, \end{aligned}$$

and one cubic correlation, that is analogous to the correlation coefficient for three random variables:

$$\begin{aligned} \rho_{123} &= \frac{\text{cov}^3(X_1, X_2, X_3)}{\sigma_1 \sigma_2 \sigma_3} \\ &= \frac{E[(X_1 - EX_1)(X_2 - EX_2)(X_3 - EX_3)]}{\sigma_1 \sigma_2 \sigma_3} \\ &= \frac{E(X_1 X_2 X_3) - p_1 p_2 p_3 - \alpha}{\sigma_1 \sigma_2 \sigma_3}, \end{aligned}$$

where $\alpha = \rho_{12} \sigma_1 \sigma_2 p_3 + \rho_{23} \sigma_2 \sigma_3 p_1 + \rho_{13} \sigma_1 \sigma_3 p_2$ and $\sigma_i = \sqrt{p_i(1-p_i)}$. The definition of Pearson correlation coefficient is extended from two variables to three variables by ρ_{123} . Then the expected value of the output Y of stochastic multiplication (AND operation) with three correlated input bit streams is derived as follows:

$$E(Y) = E(X_1 X_2 X_3) = p_1 p_2 p_3 + \rho_{123} \sigma_1 \sigma_2 \sigma_3 + \alpha. \quad (9)$$

Therefore, the computational error can be derived as:

$$\text{err}(Y) = E(Y) - p_1 p_2 p_3 = \rho_{123} \sigma_1 \sigma_2 \sigma_3 + \alpha. \quad (10)$$

The expected output and accuracy of stochastic combinational logic with multiple correlated inputs can be estimated using given probabilities and correlations in a similar manner.

III. SYNTHESIS OF TWO CORRELATED STOCHASTIC BIT STREAMS

It is necessary to synthesize two correlated bit streams with specified probabilities and correlation coefficient for simulations. In this section, we propose an approach to synthesize two stochastic bit streams with specified probabilities and correlation in unipolar representation.

Let p_1 , p_2 and ρ , respectively, represent the given probabilities of ones in the stochastic sequences X_1 , X_2 , and their correlation coefficient. Our objective is to synthesize two stochastic sequences given parameters p_1 , p_2 and ρ . The joint probability mass function (pmf) of X_1 and X_2 is described in Table II. The parameter a denotes the probability that $X_1 = 1$ and $X_2 = 1$, and can be derived from the correlation coefficient ρ . Since all values in Table II represent

TABLE II: The joint probability mass function of X_1 and X_2 .

Input Variable	Probability
$X_1 = 0, X_2 = 0$	$1 - p_1 - p_2 + a$
$X_1 = 0, X_2 = 1$	$p_2 - a$
$X_1 = 1, X_2 = 0$	$p_1 - a$
$X_1 = 1, X_2 = 1$	a

probabilities, they must be non-negative. This is guaranteed by the constraints:

$$\begin{cases} a \geq 0 \\ a \leq p_1 \\ a \leq p_2 \\ a \geq p_1 + p_2 - 1 \end{cases}$$

From the definition of the *bit-level* correlation coefficient:

$$\rho = \frac{a - p_1 p_2}{\sigma_1 \sigma_2}. \quad (11)$$

Then the parameter a can be obtained as:

$$\begin{aligned} a &= p_1 p_2 + \rho \sigma_1 \sigma_2 \\ &= p_1 p_2 + \rho \sqrt{p_1 p_2 (1 - p_1)(1 - p_2)} \end{aligned} \quad (12)$$

Note that although the correlation coefficient, ρ , lies between -1 and 1, the above constraints limit the allowable range of ρ . Since we already know $a \geq \max(0, p_1 + p_2 - 1)$ and $a \leq \min(p_1, p_2)$, the feasible range of ρ is derived as:

$$\begin{cases} \rho \geq \max\left(\frac{-p_1 p_2}{\sqrt{p_1 p_2 (1 - p_1)(1 - p_2)}}, \frac{-p_1 p_2 + p_1 + p_2 - 1}{\sqrt{p_1 p_2 (1 - p_1)(1 - p_2)}}\right) \\ \rho \leq \min\left(\frac{p_1 - p_1 p_2}{\sqrt{p_1 p_2 (1 - p_1)(1 - p_2)}}, \frac{p_2 - p_1 p_2}{\sqrt{p_1 p_2 (1 - p_1)(1 - p_2)}}\right) \end{cases} \quad (13)$$

For example, if $p_1 = 0.3$, and $p_2 = 0.8$, the range of a is constrained to the range $[0.1, 0.3]$. This limits the range of ρ to $[-0.7638, 0.3273]$. Fig. 2 shows the range of feasible

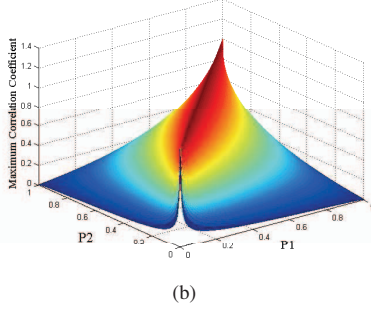
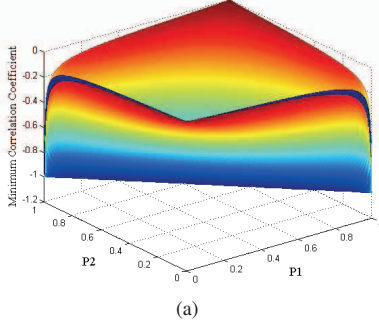


Fig. 2: (a) The minimum correlation coefficient (ρ) and (b) the maximum correlation coefficient (ρ) for all possible combinations of p_1 and p_2 .

correlation coefficient ρ for all possible combinations of p_1 and p_2 . Notice that p_1 and p_2 are in the range of $[0, 1]$.

The two correlated stochastic bit streams, X_1 and X_2 , can be synthesized from two uncorrelated bit streams, denoted as R_1 and R_2 , where each bit of R_1 and R_2 is a uniform random variable between 0 and 1. The proposed approach makes use of marginal probability and conditional marginal probability. First R_1 is used to generate X_1 using marginal probability of X_1 . Then, X_2 is generated from R_2 using conditional marginal probability of X_2 conditioned to selection of X_1 . The approach to generating X_1 follows the principle of stochastic number generator (SNG). If the probability of the first uncorrelated bit stream, R_1 , is greater than p_1 , then $X_1 = 0$, otherwise $X_1 = 1$. X_2 is synthesized by using the conditional probability of X_2 given X_1 , which is:

$$P(X_2|X_1) = \frac{P(X_1, X_2)}{P(X_1)}. \quad (14)$$

Assume that $X_1 = 1$ is given, we obtain $P(X_2 = 1|X_1 = 1) = a/p_1$. If $R_2 > a/p_1$, then $X_2 = 0$. Otherwise, $X_2 = 1$. Given that $X_1 = 0$ is generated, the conditional probability will be $P(X_2 = 1|X_1 = 0) = (p_2 - a)/(1 - p_1)$. Then $X_2 = 0$ if $R_2 > (p_2 - a)/(1 - p_1)$. Otherwise $X_2 = 1$. Fig. 3 shows the decision tree to synthesize two correlated stochastic bit streams with specified p_1 , p_2 and ρ . Every bit of two stochastic sequences is generated using this decision tree.

Fig. 4 illustrates the circuit diagram to generate two stochastic bit streams with specified probabilities and correlation coefficient. The circuit to generate two correlated stochastic signals is designed using two levels of stochastic number generator (SNG). The SNG consists of a comparator and

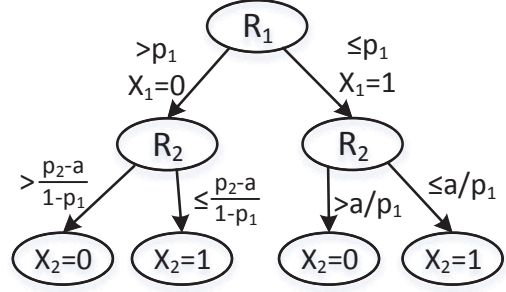


Fig. 3: The decision tree to synthesize two correlated stochastic bit streams with specified p_1 , p_2 and ρ .

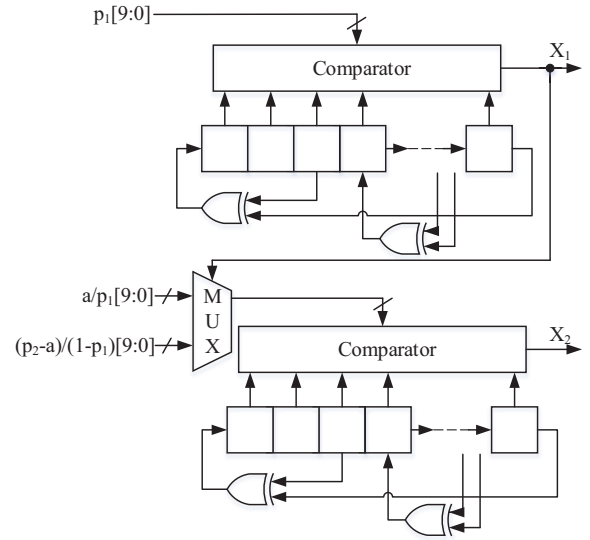


Fig. 4: The circuit diagram to generate two stochastic bit streams with specified probabilities and correlation coefficient.

a linear-feedback-shift-register (LFSR) which is a pseudo random source [12]. The first SNG is used to produce a stochastic sequence with the probability of one equal to p_1 . The binary probability number input to the second SNG is selected by using a multiplexer, where X_1 is the select signal. The second SNG is used to produce the stochastic sequence bit X_2 . The pre-computed 10-bit probabilities p_1 , a/p_1 and $(p_2 - a)/(1 - p_1)$ are inputs of the proposed architecture. X_1 and X_2 are outputs of the synthesized circuit.

IV. SYNTHESIS OF THREE CORRELATED STOCHASTIC SEQUENCES

In order to synthesize three correlated stochastic bit streams, we need to know seven parameters listed below:

$$\begin{cases} p_1 = E(X_1) \\ p_2 = E(X_2) \\ p_3 = E(X_3) \end{cases} \quad \begin{cases} \rho_{12} = \frac{\text{cov}(X_1, X_2)}{\sigma_1 \sigma_2} \\ \rho_{23} = \frac{\text{cov}(X_2, X_3)}{\sigma_2 \sigma_3} \\ \rho_{13} = \frac{\text{cov}(X_1, X_3)}{\sigma_1 \sigma_3} \\ \rho_{123} = \frac{\text{cov}_3(X_1, X_2, X_3)}{\sigma_1 \sigma_2 \sigma_3} \end{cases}$$

where p_1 , p_2 and p_3 stand for the given probabilities of each bit in the stochastic sequences X_1 , X_2 and X_3 . ρ_{12} , ρ_{23} and

ρ_{13} represent the pairwise correlations of stochastic bit streams and ρ_{123} denotes their cubic correlation. The joint probability mass function (pmf) of X_1 and X_2 and X_3 is described in Table III. The parameter a denotes the probability that $X_1 = 1$ and $X_2 = 1$, b represents the probability that $X_2 = 1$ and $X_3 = 1$, c denotes the probability that $X_1 = 1$ and $X_3 = 1$, d represents the probability that $X_1 = 1$, $X_2 = 1$ and $X_3 = 1$. These can be derived from p_1, p_2, p_3 and given correlations. Since all values in Table II represent probabilities, they must

TABLE III: The joint probability mass function of X_1, X_2 and X_3 .

$X_1 X_2$	$X_3 = 0$	$X_3 = 1$
00	$1 - p_1 - p_2 - p_3 + a + b + c - d$	$p_3 - b - c + d$
01	$p_2 - a - b + d$	$b - d$
10	$p_1 - a - c + d$	$c - d$
11	$a - d$	d

be non-negative. This is guaranteed by the constraints:

$$\begin{cases} d \geq 0 \\ d \leq \min(a, b, c) \\ p_3 + d - b - c \geq 0 \\ p_2 + d - a - b \geq 0 \\ p_1 + d - a - c \geq 0 \\ 1 - p_1 - p_2 - p_3 + a + b + c - d \geq 0 \end{cases}$$

From the definition of the bit-level correlation coefficient, the parameter a, b, c and d can be obtained as:

$$\begin{cases} a = p_1 p_2 + \rho_{12} \sigma_1 \sigma_2 \\ b = p_2 p_3 + \rho_{23} \sigma_2 \sigma_3 \\ c = p_1 p_3 + \rho_{13} \sigma_1 \sigma_3 \\ d = p_1 p_2 p_3 + \rho_{123} \sigma_1 \sigma_2 \sigma_3 + \alpha \end{cases}$$

where $\alpha = \rho_{12} \sigma_1 \sigma_2 p_3 + \rho_{23} \sigma_2 \sigma_3 p_1 + \rho_{13} \sigma_1 \sigma_3 p_2$ and $\sigma_i = \sqrt{p_i(1-p_i)}$.

The three correlated stochastic bit streams, X_1, X_2 and X_3 , can be synthesized from three uncorrelated bit streams, denoted as R_1, R_2 and R_3 , where each bit of R_1, R_2 and R_3 is a uniform random variable between 0 and 1. X_1 and X_2 are first generated by using the approach to synthesizing two correlated stochastic bit streams. In this step, parameters p_1, p_2 and a are used. In the next step, X_3 is synthesized depending on the conditional probability of X_3 given X_1 and X_2 :

$$P(X_3|X_1, X_2) = \frac{P(X_1, X_2, X_3)}{P(X_1, X_2)}. \quad (15)$$

$P(X_1, X_2, X_3)$ can be found in Table III and $P(X_1, X_2)$ is presented in Table II. Given various values of X_1 and X_2 from the first step, four cases are considered:

(i) $X_1 = 0$ and $X_2 = 0$:

$$P(X_3 = 1|X_1 = 0, X_2 = 0) = \frac{p_3 - b - c + d}{1 - p_1 - p_2 + a}.$$

If $R_3 \leq (p_3 - b - c + d)/(1 - p_1 - p_2 + a)$, then $X_3 = 1$. Otherwise, $X_3 = 0$.

(ii) $X_1 = 0$ and $X_2 = 1$:

$$P(X_3 = 1|X_1 = 0, X_2 = 1) = \frac{b - d}{p_2 - a}.$$

If $R_3 \leq (b - d)/(p_2 - a)$, then $X_3 = 1$. Otherwise, $X_3 = 0$.

(iii) $X_1 = 1$ and $X_2 = 0$:

$$P(X_3 = 1|X_1 = 1, X_2 = 0) = \frac{c - d}{p_1 - a}.$$

If $R_3 \leq (c - d)/(p_1 - a)$, then $X_3 = 1$. Otherwise, $X_3 = 0$.

(iv) $X_1 = 1$ and $X_2 = 1$:

$$P(X_3 = 1|X_1 = 1, X_2 = 1) = \frac{d}{a}.$$

If $R_3 \leq d/a$, then $X_3 = 1$. Otherwise, $X_3 = 0$.

Fig. 5 illustrates the decision tree to synthesize three correlated stochastic bit streams with specified p_1, p_2, p_3 and correlation coefficients. Every bit of three stochastic sequences is generated using this decision tree. Compared to that shown in Fig. 3, this decision tree has one more level to produce X_3 given the values of X_1 and X_2 .

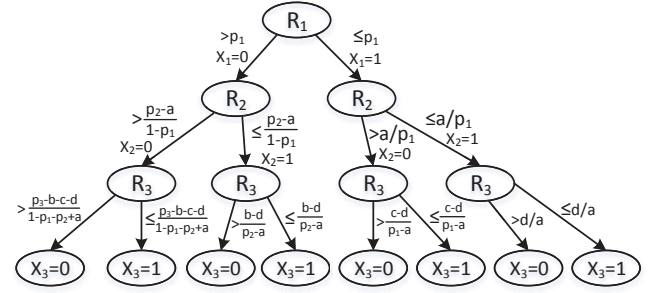


Fig. 5: The decision tree to synthesize three correlated stochastic bit streams with specified p_1, p_2, p_3 and correlation coefficients.

Fig. 6 illustrates the circuit diagram to generate three stochastic bit streams with specified probabilities and correlation coefficients. The circuit diagram to generate three correlated stochastic bit streams is similar to that shown in Fig. 4. The difference is that one more SNG is required to produce X_3 . The probability number input to the third SNG is determined by a multiplexer, where X_1 and X_2 are select signals. The pre-computed probabilities on the left side are inputs to the architecture. X_1, X_2 and X_3 are outputs of the architecture.

V. EXTENSION FOR STOCHASTIC BIPOLAR REPRESENTATION

The analysis of stochastic logic with correlated inputs and proposed synthesis circuits from Section II to Section IV are dependent on the unipolar representation. They can also be applied to bipolar representation after simple linear scaling of values represented by input sequences. For both correlation analysis of a stochastic combinational logic and the synthesis of correlated stochastic bit streams with specified parameters, we need to know the probabilities of 1s in stochastic sequences and their bit-level correlation coefficients. Consider an AND gate with the inputs of two stochastic bit streams. Given that the values represented by two sequences are n_1 and n_2 . In the context of unipolar format, we have:

$$p_1 = n_1 \text{ and } p_2 = n_2,$$

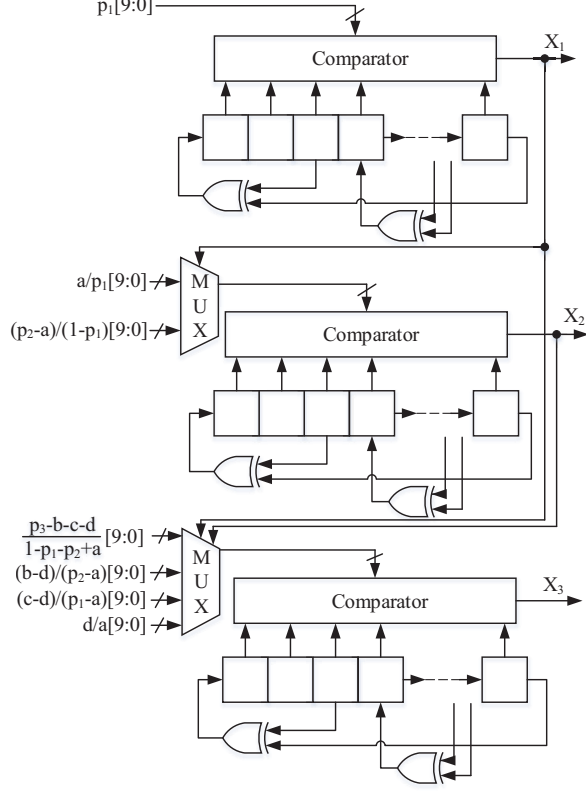


Fig. 6: The circuit diagram to generate three stochastic bit streams with specified probabilities and correlation coefficient.

where p_1 and p_2 are probabilities of 1s in two sequences respectively. However, for stochastic bipolar format:

$$p_1 = \frac{n_1 + 1}{2}$$

$$p_2 = \frac{n_2 + 1}{2}.$$

Therefore, the above linear scaling is required to derive p_i from n_i before the correlation analysis or synthesis of correlated stochastic sequences for bipolar representation. Since the bit-level correlation is defined in the context of stochastic bit streams themselves rather than the values represented by bit streams, there is no difference of the correlation coefficients between unipolar and bipolar format. In bipolar representation, besides the definition in equation (4), the correlation coefficients can also be expressed in terms of n_i as following:

$$\rho = \frac{E(X_1 X_2) - p_1 p_2}{\sqrt{p_1(1-p_1)p_2(1-p_2)}}$$

$$= \frac{\frac{n_Y+1}{2} - \frac{n_1+1}{2} \frac{n_2+1}{2}}{\sqrt{\frac{n_1+1}{2}(1 - \frac{n_1+1}{2}) \frac{n_2+1}{2}(1 - \frac{n_2+1}{2})}}$$

$$= \frac{2(n_Y + 1) - (n_1 + 1)(n_2 + 1)}{\sqrt{(n_1 + 1)(1 - n_1)(n_2 + 1)(1 - n_2)}}$$

where n_Y denotes the bipolar value represented by the output stochastic sequence of the AND gate; n_1 and n_2 are the values represented by two input bipolar stochastic sequences.

Thus, in stochastic bipolar format, we first convert n_i to p_i using linear scaling described above. Then the proposed

analysis of stochastic logic with correlated inputs and the synthesis circuits to generate correlated stochastic bit streams with specified parameters can be applied as the unipolar format.

VI. EXPERIMENTAL RESULTS

In this section, we present the test results of synthesis circuit to generate correlated bit streams. The simulation results of stochastic combinational logic with two correlated inputs are presented. We also present the synthesis results of the circuits to generate two and three stochastic bit streams with specified probabilities and correlation coefficients.

A. Test for circuit to generate correlated stochastic bit streams

1) *Synthesis circuit to generate two correlated stochastic bit streams*: The simulations were performed to test the circuit to generate two correlated stochastic bit streams with specified probabilities and correlation coefficient in *unipolar* format. Table IV shows the simulation results given distinct values of p_1 , p_2 and ρ , which are probabilities of 1s in two stochastic sequences and the correlation coefficient between them. For each combination of p_1 , p_2 and ρ , we performed 1000 Monte Carlo runs using the architecture shown in Fig. 4. The length of stochastic bit streams is 1024. The 12-bit LFSR is used as the pseudo random source with the uniform distribution, where the feedback polynomial is given as following:

$$x^{12} + x^{11} + x^{10} + x^4 + 1. \quad (16)$$

The mean values of p_1 , p_2 and ρ of generated stochastic sequences are presented as p_{1mean} , p_{2mean} and ρ_{mean} . Their standard deviations of 1000 runs are described as σ_{p_1} , σ_{p_2} and σ_ρ in Table IV.

We also performed simulations to test the circuit to generate two correlated stochastic bit streams with specified probabilities and correlation coefficient in *bipolar* format. Table V shows the simulation results given distinct values of n_1 , n_2 and ρ , which are bipolar values represented by two stochastic sequences and the correlation coefficient between them. All other experimental parameters are same as the simulations in unipolar format.

2) *Synthesis circuit to generate three correlated stochastic bit streams*: The simulation was performed to test the circuit to generate three correlated stochastic bit streams with specific probabilities and correlation coefficient in unipolar format. Given that the probabilities of 1s in three stochastic sequence are $p_1 = 0.6$, $p_2 = 0.6$ and $p_3 = 0.4$. The correlation coefficients are $\rho_{12} = -0.25$, $\rho_{23} = 0.25$, $\rho_{13} = 0.25$ and $\rho_{123} = 0.068$. We performed 1000 Monte Carlo runs using the architecture shown in Fig. 6. The length of stochastic bit streams is 1024. Three 12-bit LFSRs are used as pseudo random sources with the uniform distribution, where the feedback polynomial is the same as that in (16). We present partial results of synthesis circuit to generate three correlated stochastic bit streams in histograms. The distribution of p_1 , p_2 , p_3 and ρ_{123} of generated stochastic sequences are shown in Fig. 7, Fig. 8, Fig. 9 and Fig. 10, respectively.

TABLE IV: The simulation results of synthesis circuit to generate two correlated stochastic bit streams given distinct values of p_1 , p_2 and ρ in *unipolar* format.

Given conditions			Simulation results from synthesis circuit					
p_1	p_2	ρ	p_{1mean}	p_{2mean}	ρ_{mean}	σ_{p_1}	σ_{p_2}	σ_ρ
0.2	0.4	0.05	0.2003	0.3998	0.0480	0.0111	0.0136	0.0314
0.2	0.4	0.15	0.1996	0.3990	0.1504	0.0106	0.0135	0.0317
0.3	0.5	0.15	0.2998	0.4993	0.1511	0.0120	0.0140	0.0306
0.3	0.5	0.25	0.2993	0.4997	0.2504	0.0127	0.0140	0.0279
0.4	0.6	0.25	0.3999	0.6003	0.2506	0.0126	0.0133	0.0288
0.4	0.6	0.35	0.3994	0.5996	0.3499	0.0132	0.0142	0.0264
0.5	0.7	0.35	0.5007	0.7002	0.3495	0.0133	0.0125	0.0259
0.5	0.7	0.45	0.4997	0.6999	0.4499	0.0134	0.0134	0.0247
0.6	0.8	0.45	0.6005	0.7999	0.4489	0.0128	0.0113	0.0252
0.6	0.8	0.55	0.5992	0.7997	0.5488	0.0134	0.0117	0.0219

TABLE V: The simulation results of synthesis circuit to generate two correlated stochastic bit streams given distinct values of n_1 , n_2 and ρ in *bipolar* format.

Given conditions			Simulation results from synthesis circuit					
n_1	n_2	ρ	n_{1mean}	n_{2mean}	ρ_{mean}	σ_{n_1}	σ_{n_2}	σ_ρ
-0.6	-0.2	0.05	-0.5995	-0.2021	0.0518	0.0213	0.0254	0.0317
-0.6	-0.2	0.15	-0.6002	-0.1998	0.1487	0.0213	0.0274	0.0322
-0.4	0	0.15	-0.3995	-0.0013	0.1499	0.0250	0.0277	0.0310
-0.4	0	0.25	-0.3997	-0.0007	0.2503	0.0251	0.0289	0.0294
-0.2	0.2	0.25	-0.2009	0.1999	0.2504	0.0270	0.0269	0.0282
-0.2	0.2	0.35	-0.2000	0.1999	0.3499	0.0269	0.0278	0.0272
0	0.4	0.35	0.0001	0.4005	0.3513	0.0278	0.0252	0.0274
0	0.4	0.45	0.0009	0.3997	0.4500	0.0273	0.0259	0.0242
0.2	0.6	0.45	0.2011	0.6009	0.4488	0.0263	0.0230	0.0248
0.2	0.6	0.55	0.1994	0.5998	0.5485	0.0253	0.0222	0.0214

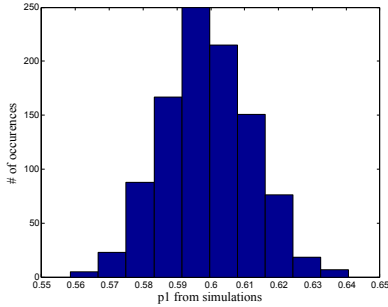


Fig. 7: The histogram of the mean value (p_1) of the first stochastic bit stream generated from the synthesis circuit where the expected $p_1 = 0.6$.

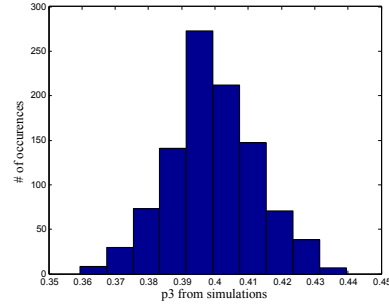


Fig. 9: The histogram of the mean value (p_3) of the third stochastic bit stream generated from synthesis circuit where the expected $p_3 = 0.4$.

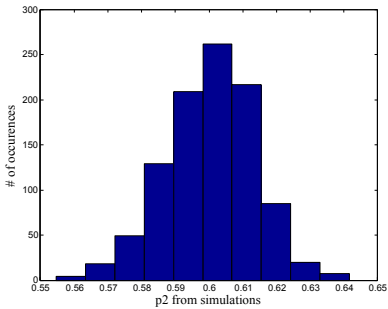


Fig. 8: The histogram of the mean value (p_2) of the second stochastic bit stream generated from the synthesis circuit where the expected $p_2 = 0.6$.

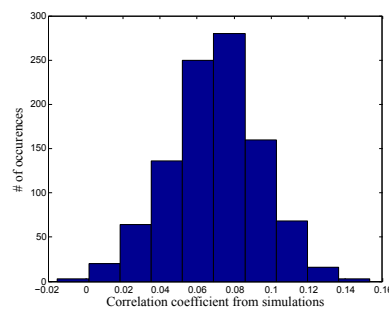


Fig. 10: The histogram of the correlation coefficient (ρ_{123}) of the stochastic bit streams generated from synthesis circuit where the expected $\rho_{123} = 0.068$.

B. Simulation results of stochastic logic with correlated inputs

In our simulations, the results of output for two-input logic gates with correlated stochastic inputs are obtained using Monte Carlo experiments for different values of p_1 and p_2 , which are probabilities of 1s in two correlated stochastic inputs. 1000 Monte Carlo runs were performed for each combination of p_1 , p_2 and ρ . The length of stochastic bit streams is 1024. The correlated input stochastic bit streams are generated by proposed synthesis circuits. Table VI presents the output mean values and standard deviations of different combinational logic gates given specified p_1 , p_2 and ρ of input stochastic sequences. The output and standard deviation results from

TABLE VI: The output mean values and standard deviations of different combinational logic gates given specified p_1 , p_2 and ρ of input stochastic sequences.

Gate Type	Input			Output			
	p_1	p_2	ρ	p_{out}	p_{pred}	σ_{out}	σ_{pred}
AND	0.4	0.5	0.2	0.2490	0.2489	0.0133	0.0135
	0.6	0.8	0.5	0.5778	0.5780	0.0156	0.0154
OR	0.4	0.5	0.2	0.6512	0.6510	0.0144	0.0149
	0.6	0.8	0.5	0.8217	0.8220	0.0118	0.0120
XNOR	0.4	0.5	0.2	0.5978	0.5980	0.0159	0.0153
	0.6	0.8	0.5	0.7560	0.7560	0.0131	0.0134

simulations are represented by p_{out} and σ_{out} . p_{pred} and σ_{pred} indicate our predicted mean values and standard deviations of the output. p_{pred} is calculated by using expressions shown in Table I. The predicted standard deviations are calculated using $\sqrt{p_Y(1-p_Y)/N}$ where $N = 1024$. N represents the length of stochastic sequence. The simulation results in Table VI are in agreement with the predicted values.

We also performed simulations for a 3-input AND gate with correlated stochastic inputs. Given $p_1 = 0.6$, $p_2 = 0.6$, $p_3 = 0.4$, $\rho_{12} = -0.25$, $\rho_{23} = 0.25$, $\rho_{13} = 0.25$ and $\rho_{123} = 0.068$, three correlated stochastic sequences are generated using proposed synthesis circuit shown in Fig. 6. 1000 Monte Carlo runs were performed to test the output values and standard deviations. From simulations, we obtain:

$$\begin{cases} p_{out} = 0.1993 \\ \sigma_{out} = 0.0126 \end{cases}$$

The predicted output mean value, $p_{pred} = 0.2$, is calculated by using equation (9). The predicted standard deviation is computed using $\sqrt{p_Y(1-p_Y)/N}$, where $\sigma_{pred} = 0.0125$.

C. Synthesis results

The hardware complexity and power consumption of proposed architectures for synthesizing correlated stochastic bit streams (Fig. 4 and Fig. 6) are evaluated using 65nm technology. After successful FPGA verification, the architectures are implemented using 65nm libraries and synthesized using Synopsys Design Compiler. In our implementation, the length of the stochastic sequence is 1024, thus the LFSR requires at least 10 bits. Table VII presents the hardware complexity in terms of equivalent 2-NAND gates and power consumption of circuits to generate two stochastic bit streams (corr2) and three stochastic bit streams (corr3) with specified probabilities and correlation coefficients.

TABLE VII: The hardware complexity in terms of equivalent 2-NAND gates and power consumption of circuits to generate two and three stochastic bit streams with specified probabilities and correlation coefficients.

Circuit Type	SNG*	corr2		corr3	
	Simulated	Simulated	Overhead	Simulated	Overhead
Area	188.76	411.84	9.09%	685.36	21.03%
Power	1.18 μ W	2.41 μ W	2.12%	3.71 μ W	4.80%

*The synthesis results of SNG is presented as a reference.

The area and power overheads for two correlated bit streams are 9.09% and 2.12%, respectively, and for three correlated bit streams are 21.03% and 4.80%, respectively.

VII. CONCLUSION

This paper has presented the analysis of stochastic logic gates with correlated inputs. Approaches to generating two and three correlated bit streams have been proposed. A major weakness of the proposed approach is that the correlation coefficient of the two bit streams does not span the entire range from -1 to 1. Future work will be directed towards generation of correlated bit streams where the correlation coefficient can range from -1 to 1.

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